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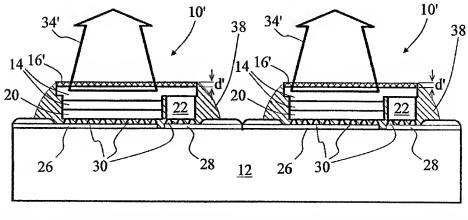
(54) Title: LASER LIFT-OFF OF SAPPHIRE FROM A NITRIDE FLIP-CHIP




(57) Abstract: In a method for fabricating a flip-chip light emitting diode device, epitaxial layers are deposited on a sapphire growth substrate to produce an epitaxial wafer. A plurality of light emitting diode devices are fabricated on the epitaxial wafer. The epitaxial wafer is diced to generate a device die. The device die is flip chip bonded to a mount. The flip chip bonding includes securing the device die to the mount by bonding at least one electrode of the device die to at least one bonding pad of the mount. Subsequent to the flip chip bonding, the growth substrate of the device die is removed via the application of laser light.

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# LASER LIFT-OFF OF SAPPHIRE FROM A NITRIDE FLIP-CHIP

## BACKGROUND

The present invention relates to the electronics arts. It is especially relates to group III-nitride flip-chip bonded light emitting diodes for lighting applications, and will be described with particular reference thereto. However, the invention also finds application in conjunction with other types of flip-chip bonded light emitting diodes, and in other flip-chip bonded epitaxial semiconductor devices such as vertical cavity surface emitting laser diodes.

In the flip-chip mounting configuration, a light emitting diode with a light-transmissive substrate and front-side electrodes is bonded "face down" to bonding bumps of a mount, that is, with the epitaxial layers proximate to the mount and the light-transmissive substrate distal from the mount. The flip-chip arrangement has a number of advantages, including improved thermal heat sinking due to the proximity of the front-side active layers to the heat sinking substrate, and reduction of electrode shadowing losses.

In the flip-chip mounting configuration, light is extracted from the substrate side. For epitaxially grown light emitting diodes, the choices for substrate material can be highly restricted since the substrate is selected principally to provide a good base for the epitaxy. Thus, the substrate criteria include a narrow lattice constant range, a substantially atomically flat surface for nucleation of epitaxy, thermal stability at epitaxial growth temperatures, chemical compatibility with the epitaxial process, and so forth.

A problem can arise in the flip-chip configuration when the growth substrate is substantially light-absorbing over some or all of the spectral range of light emission. In this case, light extraction from the substrate is reduced due to light absorption losses in the substrate. Moreover, even if a suitable optically transparent substrate is available, such as is the case for group III-nitride light emitting diodes which can be grown on a transparent sapphire growth substrate, reflection optical losses can occur at the interface between the

substrate and the epitaxial layers due to an abrupt discontinuity in refractive index.

A known approach for reducing these substrate-related optical losses is to transfer the epitaxial layers stack from the light-absorbing growth substrate wafer to an optically transparent wafer. Typically, this involves intimately bonding the epitaxial layers stack to the optically transparent wafer, and then removing the growth substrate wafer by etching. After removal of the growth substrate, the epitaxial layers stack remains bonded to the transparent wafer, which is then processed to fabricate devices, and diced to separate individual light emitting diode die. However, achieving intimate bonding between the epitaxial layers stack and the transparent substrate over large areas is difficult. Device yield can be compromised due to the formation of air bubbles or the presence of particles at the interface between the epitaxial layers stack and the transparent substrate during the bonding. Moreover, absent a close refractive index match between the epitaxial layers stack and the transparent substrate, reflections at the interface between the layers stack and the transparent wafer can introduce optical losses.

Another approach is to temporarily secure the epitaxial layers stack to a temporary support wafer using an adhesive layer, followed by thinning of the growth substrate. The epitaxial layers stack, with the remaining thinned growth substrate adhering thereto, is then detached from the temporary support wafer and processed and diced to produce light emitting diode die. The light emitting diode die, which have thinned substrates, are flip chip bonded to a mount. However, the epitaxial layers stack and the remaining thinned growth substrate form a fragile structure after growth substrate thinning. The fragility of this thinned structure complicates the further processing, dicing, and flip chip bonding, resulting in lowered device yield. Moreover, air bubbles, particles, or other imperfections in the adhesion between the temporary support wafer and the epitaxial layers stack can introduce localized damage to the thinned structure, also impacting device yield.

The present invention contemplates an improved apparatus and method that overcomes the above-mentioned limitations and others.

## BRIEF SUMMARY

According to one embodiment, a method is provided for fabricating a flip-chip light emitting diode device. Epitaxial layers are deposited on a growth substrate to produce an epitaxial wafer. A plurality of light emitting diode devices are fabricated on the epitaxial wafer. The epitaxial wafer is diced to generate a device die. The device die is flip chip bonded to a mount. The flip chip bonding includes securing the device die to the mount by bonding at least one electrode of the device die to at least one bonding pad of the mount. Subsequent to the flip chip bonding, a thickness of the growth substrate of the device die is reduced.

According to another embodiment, a method is provided for improving light emission of a flip-chip bonded light emitting diode device that is flip chip bonded to a mount. A growth substrate of the light emitting diode device is thinned or removed. The growth substrate of the flip-chip bonded light emitting diode device is arranged distal from the mount. The thinning or removing is performed while epitaxial layers of the light emitting diode device are flip chip bonded to the mount. The flip chip bonding effects a securing of the light emitting diode device to the mount during the thinning or removing.

According to yet another embodiment, a flip-chip light emitting diode device is disclosed. A mount includes bonding bumps. A light emitting diode device die has a device layers stack that is flip chip bonded to the bonding bumps of the mount. An underfill material is arranged between the light emitting diode device die and the mount. The underfill material supports the light emitting diode device die and prevents the light emitting diode device die from fracturing.

Numerous advantages and benefits of the present invention will become apparent to those of ordinary skill in the art upon reading and understanding the present specification.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may take form in various components and arrangements of components, and in various process operations and arrangements of process operations. The drawings are only for purposes of illustrating preferred embodiments and are not to be construed as limiting the invention. In the cross-sectional views, layer thicknesses are exaggerated for visual clarity, and are therefore not drawn to scale.

FIGURE **1A** shows a cross-sectional view of two light emitting diode dice flip chip bonded to a mount.

FIGURE **1B** shows a cross-sectional view of the two light emitting diode dice flip chip bonded to the mount as in FIGURE **1A**, after thinning of the substrates of the two light emitting diode dice.

FIGURE **2** plots calculated light extraction fraction values of a group III-nitride flip-chip light emitting diode die having a silicon carbide substrate, calculated as a function of substrate absorption coefficient and substrate thickness.

FIGURE **3** shows a cross-sectional view of the two light emitting diode dice flip chip bonded to the mount as in FIGURE **1A**, after removal of the substrates of the two light emitting diode dice.

FIGURE **4A** shows a cross-sectional view of two light emitting diode dice having a vertical current flow geometry flip chip bonded to a mount, prior to substrate thinning and formation of a back-side electrode.

FIGURE **4B** shows a cross-sectional view of the two light emitting diode dice flip chip bonded to the mount as in FIGURE **4A**, after thinning of the substrates, formation of back-side electrodes, and wire-bonding of the back-side electrodes to wiring bonding pads of the mount.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference to FIGURE **1A**, two exemplary flip chip bonded light emitting diode device die **10** are shown mounted in flip-chip fashion on a mount **12**. Each exemplary light emitting diode device die **10** includes a

semiconductor device layers stack **14** that is epitaxially deposited on a growth substrate **16**. The epitaxial device layers stack **14** defines a light emitting diode device such as a group III nitride ultraviolet or blue light emitting diode, a group III phosphide visible-emission light emitting diode, a group III arsenide vertical cavity surface emitting laser diode, or the like.

In FIGURE **1A**, the semiconductor layers stack **14** has two exemplary layers corresponding to a simple p/n diode; however, those skilled in the art will appreciate that more complex semiconductor layers stacks can be employed. In a vertical cavity surface emitting laser diode, for example, the layers stack can include dozens of layers that define Bragg reflectors, claddings, and a complex multi-quantum well active region. For a group III nitride ultraviolet or blue light emitting diode with a p-on-n orientation, the layers stack typically includes an epitaxial growth buffer of aluminum nitride or another material, an n-type gallium nitride base layer, an active region of indium gallium nitride, a p-type gallium nitride layer, and optionally a contact layer formed on the p-type gallium nitride layer. Those skilled in the art can readily construct other semiconductor epitaxial layers stacks that are suitable for specific optical applications.

The growth substrate **16** is made of a crystalline material that is suitable for epitaxial growth of the selected semiconductor layers stack **14**. For group III nitride epitaxy, the growth substrate is suitably silicon carbide (SiC; for example, conductive SiC, undoped 6H-SiC, or undoped 4H-SiC), gallium nitride, or sapphire. For group III phosphide epitaxy, the growth substrate is suitably gallium arsenide or indium phosphide. For group III arsenide epitaxy, the substrate is suitably gallium arsenide. These examples are not exhaustive; rather, those skilled in the art can readily select a growth substrate having a suitable surface lattice constant, a large-area planar surface, and appropriate thermal and chemical characteristics for promoting high quality, preferably lattice-matched epitaxial growth of the selected semiconductor layers stack **14**. Optionally, the growth substrate **16** is off-cut relative to a principle crystal direction. For example, 4H-SiC substrates that are on-axis (that is, no offcut) or offcut at 4° or 8° are available from Cree Materials (Durham, North Carolina).

Epitaxial deposition of the semiconductor layers stack **14** on the selected growth substrate **16** is preferably by metal-organic chemical vapor deposition (MOCVD; also known in the art as organometallic vapor phase epitaxy, OMVPE, and similar nomenclatures), molecular beam epitaxy (MBE), liquid phase epitaxy (LPE), or another suitable epitaxial growth technique. As with the growth substrate **16**, the choice of epitaxial growth technique is made based on the type of epitaxial layer stack **14** that is to be grown.

The epitaxial deposition is performed over a large-area substrate wafer. For example, silicon carbide wafers for epitaxy are available as generally disk-shaped wafers of diameter about 5 cm to 8 cm in diameter. Gallium arsenide and sapphire are available as larger diameter disk-shaped wafers. The large-area substrate wafer with the epitaxial layers stack **14** deposited thereupon is referred to herein as an epitaxial wafer. The epitaxial wafer is processed using a suitable fabrication process including sub-processes such as wafer cleaning processes, lithography processes, etching processes, dielectric deposition processes, metallization processes, and the like to define a plurality of light emitting diode devices on the wafer. In a typical approach, the fabrication process includes initial wafer cleaning, lithographic definition and etching of device mesas, and lithographic definition and formation of n-type and p-type electrodes.

With continuing reference to FIGURE **1A**, the light emitting diode device die **10** are lateral current flow geometry devices, and include a p-type electrode **20** disposed on the device mesa and an n-type electrode **22** disposed in a field area off the device mesa. In this embodiment, both electrodes **20**, **22** are front-side electrodes. Typically, the electrodes **20**, **22** are made of gold or have gold coatings for facilitating low-resistance electrical contact.

The mount **12** includes a first bonding pad **26** arranged to connect with the p-type electrode **20**, and a second bonding pad **28** arranged to connect with the n-type electrode **22**. A plurality of bonding bumps **30** are arranged on the bonding pads **26**, **28**. The light emitting diode device die **10** are flip chip bonded to the bonding pads **26**, **28** of the mount **12**, and more

specifically bond to the bonding bumps **30**. Flip chip bonding can be achieved by soldering, in which case the bonding bumps **30** are solder bumps. Alternatively, flip chip bonding can be achieved by thermosonic bonding, in which case the bumps are preferably gold-coated copper bumps that are bonded to the gold of the electrodes **20**, **22** by a combination of heating and injection of ultrasonic energy. Other bonding methods can also be employed.

With continuing reference to FIGURE **1A**, the flip chip bonded light emitting diode die **10** have substrates **16** that are relatively thick. The growth substrate wafer, which is typically at least a few centimeters in diameter or other lateral dimension, is diced to generate the individual light emitting diode die **10** that are flip chip bonded to the mount **12**. Hence, the substrates **16** of FIGURE **1A** have a thickness **d** corresponding to the thickness of the original growth substrate wafer. For example, standard disk-shaped silicon carbide wafers for group III-nitride epitaxy available from Cree Materials (Durham, North Carolina) have typical wafer diameters of around 5.0 cm to 7.6 cm, and have wafer thicknesses specified as $254 \pm 25.4$ microns.

Moreover, silicon carbide is absorbing for the ultraviolet to blue light emission of typical group III-nitride light emitting diode devices. In the flip chip bonding arrangement, light extraction is typically through the substrate side, and is attenuated by substrate absorption. In FIGURE **1A**, extracted light is indicated schematically by tapered arrows **34**. A rapid tapering of the arrow **34** as it passes through the relatively thick light absorbing substrate **16** is indicative of optical losses due to light absorption. Although described with reference to a silicon carbide substrate, it will be appreciated that other substrates that are absorbing for light emitted by the semiconductor layers stack will similarly absorb light and reduce the external light output of the device.

With continuing reference to FIGURE **1A** and with further reference to FIGURE **1B**, the substrate **16** shown in FIGURE **1A** is thinned after the flip chip bonding to produce modified light emitting diode die **10'** that have thinned substrates **16'**, as shown in FIGURE **1B**. The thinned substrate **16'** has a thickness **d'** indicated in FIGURE **1B** that is substantially less than

the thickness **d** of the unthinned substrate **16**. The substrate thinning can be performed by mechanical lapping, mechanical polishing, mechanical grinding, or the like. In another approach, the wafer thinning is performed by wet etching or dry chemical or plasma etching using a suitable etchant. In yet another approach, laser ablation is used to thin the substrate. The reduced thickness **d'** of the thinned substrate **16'** allows more light to exit the light emitting diode die **10'**, as indicated by less tapered, that is, broader arrows **34'** shown in FIGURE **1B**.

A preferred amount of thinning, that is, a preferred final thickness **d'**, is determined based on several factors. As a light-absorbing substrate is thinned, it generally becomes more light transmissive. Hence, a smaller thickness **d'** typically promotes light extraction. However, a smaller final thickness **d'** implies a smaller tolerance in the thinning process. In other words, for a smaller final thickness **d'**, the substrate thinning process should be more precisely controlled to avoid leaving too much substrate material, on the one hand, or removing too much material and possibly damaging the underlying epitaxial layers stack **14**, on the other hand.

With reference to FIGURE **2**, calculated light extraction values for a typical group III-nitride device structure on silicon carbide substrates of different thicknesses and absorption characteristics is shown. In the plot of FIGURE **2**, the abscissa is the substrate thickness in microns, and the ordinate is light extraction fraction. Calculations are shown running from a typical silicon carbide growth wafer thickness of 254 microns down to a highly thinned substrate thickness of about 25.4 microns. Several curves are shown, each corresponding to a different substrate absorption coefficient $\alpha$, ranging from $\alpha$=0.0 $cm^{-1}$ to $\alpha$=20.0 $cm^{-1}$. Those skilled in the art will appreciate that the absorption coefficient is wavelength dependent, and in the case of silicon carbide also depends upon the polymorph, doping, and other characteristics of the silicon carbide material. The range of absorption coefficients plotted in FIGURE **2** is representative of substrate absorption characteristics for typical group III-nitride light emitting diode device emission wavelengths and for typical silicon carbide substrate materials.

With continuing reference to FIGURE **2**, for $\alpha$=5.0 $cm^{-1}$, thinning from a substrate thickness of 254 microns to a substrate thickness of 50.8 microns provides a relative light extraction improvement of about 10.2% (from a light extraction fraction of 0.2224 to a light extraction of 0.2451). For a higher absorbing substrate the improvement is larger. For example, in the case of $\alpha$=20.0 $cm^{-1}$, the light extraction fraction is 0.1212 for a 254 micron substrate, and increases to 0.1918 for a 25.4 micron substrate. Thus, in the case of $\alpha$=20.0 $cm^{-1}$, thinning from 254 microns to 25.4 microns provides a relative light extraction improvement of about 58.3%.

With reference returning to FIGURES **1A** and **1B**, thinning the substrate **16** after flip chip bonding, rather than before dicing as has been typically done in the past, can introduce mechanical stability difficulties, especially for thinned substrates **16'** having thicknesses **d'** of about 50 microns or less. Stresses introduced by the bonding or by the substrate thinning process can result in some, most, or all of the light emitting diode devices **10'** being operatively degraded or non-functional. For example, some, most, or all of the light emitting diode devices **10'** can break during the thinning process due to stresses introduced at the discrete bonding areas corresponding to the bonding bumps **30**. Such stresses may be supportable by the light emitting diode die **10** due to its thick substrate **16** and corresponding mechanical robustness, but may be unsupportable by the light emitting diode die **10'** because of the fragility of its thinned substrate **16'**.

To mechanically support and stabilize the light emitting diode devices during and after thinning, an underfill material **38** is preferably disposed between the light emitting diode device **10** and the mount **12** prior to substrate thinning. The underfill material **38** provides adhesive bonding between the light emitting diode device **10, 10'** and the mount **12** that helps secure the devices **10, 10'**. The underfill material **38** also provides mechanical support for the thinned light emitting diode device **10'** to reduce a likelihood of cracking or other stress-related damage. The support provided by the underfill material **38** is distributed across the area of the light emitting diode device **10,**

**10'** to provide support at or proximate to localized stress regions such as at or around the bonding bumps **30**.

The underfill material **38** preferably provides other benefits, such as protection and encapsulation of the semiconductor layers stack **14** and electrodes **20**, **22**. If the underfill material **38** is thermally conductive, it advantageously provides an additional heat sinking path.

To provide for the thinning of the substrate, the underfill material **38** preferably substantially does not cover the substrate **16**, although the underfill material **38** optionally can come part-way up sides of the substrate **16**. In some contemplated embodiments, the underfill material does cover the substrate **16**, and the excess material covering the substrate **16** is removed during the substrate thinning process. The underfill material **38** is suitably applied as a fluid and then cured or dried before or after bonding. The underfill material **38** is suitably an epoxy, silicone, photoresist, or other material that can be applied in a liquid or flowable form and then cured or dried. Although inclusion of the underfill material **38** is preferred, the underfill material **38** is optionally omitted if the thickness **d'** of the thinned substrate is above about 50 microns, or if the epitaxial layers stack **14** is sufficiently mechanically strong to be resistant to stress-related damage.

In the case of group III-nitride light emitting diode devices that emit blue or ultraviolet light, a wavelength converting phosphor can be incorporated into the underfill material **38** to convert the blue or ultraviolet light into white light or light having other selected spectral characteristics. Such phosphor incorporation is most beneficial in devices that employ a lateral current flow geometry, such as the light emitting diode device die **10**, **10'**, since in this geometry a substantial amount of light leaks toward the mount **12** through sidewalls of the etched mesa.

With reference to FIGURE **3**, rather than thinning the substrate **16** of FIGURE **1A**, the substrate **16** can be completely removed, as shown in FIGURE **3**, to produce the modified flip chip light emitting diode die **10"**. In the case of a transparent substrate such as a sapphire substrate used in group III-nitride epitaxy, optical losses attributable to the substrate are due to reflection

losses rather than absorption losses. Hence, the sapphire should be entirely removed to obviate the reflection optical losses. In one suitable embodiment, a chemical etching is used that removes the substrate material selectively over the material of the adjacent epitaxial layer. In this case, the epitaxial layer of the epitaxial layers stack **14** that is adjacent to the substrate **16** serves as an etch stop, and the chemical etching advantageously terminates or greatly slows when it reaches the etch stop layer.

In another embodiment, an excimer laser is used to remove a sapphire substrate **16** from a flip-chip mounted LED die. One advantage of laser lift-off of the sapphire substrate is that better light extraction can be achieved. Additionally the resulting lower profile provides more options for further packaging. The process of flip-chip mounting can involve relatively large amounts of force that may tend to damage the die. Accordingly, removing the substrate after the chip has been flip-chip mounted (as opposed to before mounting) helps prevent damage to the die during the mounting process insomuch as the then intact substrate provides additional structural support and/or integrity. In addition, there is a built up stress in the device layer because of the lattice mismatch between the sapphire substrate and the device layer which could cause the chip to "curl" upon removal of the substrate. Depending on the size of the chip and the degree of curl, a stress relief agent such as the underfill **38** is applied to the die before removal of the sapphire substrate. If there is relatively little curl in the device layer after the substrate has been removed, the use of another agent to prevent external damage is optionally implemented.

Removing the sapphire substrate from the active region or epitaxial layers **14** of the device has certain challenges. Once the sapphire is removed, the integrity and robustness of the chip is can be comparatively low because the remaining device is only on the order of 10μm thick as opposed to 100-600μm with the substrate. The removal of the substrate from a singlated device proves to be a more advantageous process as compared to removing the entire substrate at the larger wafer level because of the nature of the laser lift-off process. Suitably, ultraviolet laser light is illuminated on the back surface

or substrate side surface of the epitaxial layers **14** through the transparent sapphire substrate. The laser light degrades the interface between the sapphire and a low-quality AlGaN or GaN nitride nucleation layer that has been formed to ease the lattice mismatch between the materials. During this degradation, gallium metal and nitrogen are released. Then, at slightly elevated temperature, the gallium melts and allows the sapphire to be removed. The surface is then cleaned of any remaining gallium.

As already mention, before the laser lift-off process, the die can be secured to a submount or underlying support structure with either an underfill of epoxy or other material, e.g., that is not electrically active but can provide support to the chip after the substrate is removed. If the distance between the die and underlying support structure is small, a coating material that could be removed later is optionally used to provide temporary support. This could also be an epoxy, but it would not have to flow underneath the chip, just around the edges. Of course, after lift-off, more options exist to treat the flip-chip mounted die to both provide additional strength and also enhance the performance of the device, e.g., an anti-reflection coating may be used to enhance light output from the device; depositing an index-graded film on the chip that would change the total internal reflection and allow for more light output as well, notably, GaN has an index of refraction around 2.3 and epoxy has an index of refraction around 1.5, accordingly materials having indicies or refraction between these two are suitably used; a micro-lenses is optionally deposited on the backside of the die; roughening or etching the backside of the die into lenses or other structures is optionally performed; an injection transfer molding process may be carried out to form a large lens over the chip (e.g., the lens is optionally initially a liquid that is harden or alternately the lens may be solid initially); etc.

Typically, complete removal of the substrate **16** provides improved light extraction efficiency compared with retaining the thinned substrate **16'**. However, if the substrate **16'** provides good refractive index matching to the outside ambient, the thinned substrate **16'** can provide better overall light extraction efficiency than is obtained with complete substrate

removal. Moreover, complete substrate removal leaves a layer of the epitaxial layers stack **14** exposed to the ambient. In certain cases, this may be undesirable. For example, in a group III-arsenide device grown on a gallium arsenide substrate, if the exposed epitaxial layer has a high aluminum content, it is prone to oxidation. Thus, in such a case it may be preferable to keep a thin portion of the gallium arsenide substrate to cap the high aluminum-content epitaxial layer. Still further, absent an etch stop layer or a thick non-critical base epitaxial layer, complete removal of the substrate **16** involves very precise control of the etch process to avoid etching into and damaging the thin epitaxial layers stack **14**.

In the case of removal or substantial thinning of the substrate **16**, the resultant light emitting diode device **10'**, **10"** may be so fragile as to be incapable of being a free-standing component. That is, in the case of extreme thinning or removal of the substrate **16**, the underfill material **38** advantageously prevents fracture of the light emitting diode device **10'**, **10"**. Whether or not the modified light emitting diode device **10'**, **10"** is so fragile that the underfill material **38** prevents its fracture, rather than merely providing additional mechanical support, depends upon the thickness of the epitaxial layers stack **14**, the thickness **d'** of the thinned substrate **16'** in the case of incomplete substrate removal, and the mechanical properties of the materials that make up the light emitting diode device **10'**, **10"**.

With continuing reference to FIGURE **3**, an index-matching material, an epoxy lens, discrete microlens, or other optical element **42** can be applied to the epitaxial layer stacks **14** after removal of the substrates **16**. In the case of an epoxy lens **42**, the epoxy is typically applied in liquid or flowable form and then dried or cured. Although not shown, it will be appreciated that such optical elements can also be disposed on the thinned substrates **16'** of FIGURE **1B**.

With reference to FIGURE **4A**, an embodiment employing devices having a vertical current flow geometry is described. Light emitting diode die **100** are shown in FIGURE **4A** flip-chip bonded to a mount **112**. The light emitting diode die **100** have an epitaxial semiconductor device layers

stack **114** disposed on a substrate **116**. A first electrode **120** is formed on the device layers stack **114**. Unlike the lateral current flow geometry of FIGURES **1A**, **1B**, and **3**, only a single front-side electrode **120** is formed on the epitaxial layers stack **114**. The first electrode **120** is flip-chip bonded to a first bonding pad **126** via bonding bumps **130**. A second bonding pad **128** is not connected to the light emitting diode die **100** by flip chip bonding. Thus, at the point in fabrication shown in FIGURE **4A**, the light emitting diode die **100** are inoperative since there is no second electrode or electrical input thereto to drive the diode device.

With continuing reference to FIGURE **4A** and with further reference to FIGURE **4B**, an underfill material **138** is preferably disposed between the light emitting device die **100** and the mount **112** to provide mechanical support, improved securing of the device die **100** to the mount **112**, and to provide optional encapsulation and improved heat sinking. The substrate **116** shown in FIGURE **4A** is thinned by mechanical grinding, laser ablation, wet chemical etching, dry etching, or the like to produce the thinned substrate **116'**. A second electrode **122**, which is a back-side electrode, is formed on the thinned substrate **116**, which is an electrically conductive substrate. In the illustrated embodiment, the second electrode **122** is a ring electrode that defines a central optical aperture **140** of each modified light emitting diode die **100'**. The second electrode **122** is electrically connected with the second bonding pad **128**, which is a wiring bonding pad, by a wire bond **142**. When energized by the electrodes **120**, **122** the modified light emitting diode die **100'** emits light **134** passing through the thinned substrate **116'** within the optical aperture **140**.

In the exemplary embodiment of FIGURE **4B**, the thinned substrate **116'** is electrically conductive to enable a vertical current flow configuration. If, however, the substrate is electrically insulating, for example a sapphire substrate of a group III-nitride light emitting diode die, then the substrate can be completely removed analogously to the embodiment of FIGURE **3**, followed by formation of the backside contact on a layer of the

semiconductor layers stack **114** that is exposed by the removal of the substrate **116**.

By removing the substrate after flip chip bonding, a number of advantages are realized over past fabrication methods that performed wafer thinning prior to flip chip bonding. Fabrication processes for making the individual light emitting diode device die are performed on an epitaxial wafer that has a thick substrate wafer. This avoids damage during handling of thin-wafer devices, and thus improves device yield. Moreover, in the case of substrate removal by isotropic etching with an etch stop, performing such isotropic etching after dicing and flip-chip bonding allows the isotropic etch process to simultaneously remove material from both the back and the sides of the substrate wafer **16, 116**. This can provide faster substrate removal, especially in the case of small-area devices. Moreover, inclusion of a supportive underfill material **38, 138** provides improved structural stability during and after the substrate thinning or removal process, again increasing yield. In certain embodiments, the supportive underfill material **38, 138** prevents mechanical failure and enables substrate thinning or removal to produce devices that cannot be generated as free-standing components.

The invention has been described with reference to the preferred embodiments. Obviously, modifications and alterations will occur to others upon reading and understanding the preceding detailed description. It is intended that the invention be construed as including all such modifications and alterations insofar as they come within the scope of the appended claims or the equivalents thereof.

WHAT IS CLAIMED IS:

CLAIMS

1. A method for fabricating a flip-chip light emitting diode device, the method including:

(a) depositing epitaxial layers on a growth substrate to produce an epitaxial wafer;

(b) fabricating a plurality of light emitting diode devices on the epitaxial wafer;

(c) dicing the epitaxial wafer to generate at least one separated device die from the epitaxial wafer, said device die including at least one of the plurality of the light emitting diode devices and a portion of the growth substrate;

(d) flip chip bonding the device die to a mount, said flip chip bonding including securing the device die to the mount by bonding an electrode of the device die to a bonding pad of the mount; and,

(e) subsequent to step (d), removing at least some of the growth substrate from the device die.

2. The method of claim 1, further comprising:

(f) prior to step (e), providing a support material that supports the device die relative to the mount.

3. The method of claim 2, wherein step (f) comprises:

providing the support material in a flowable form that contacts the device die and the mount; and,

hardening the support material into a non-flowable form.

4. The method of claim 2, further comprising:

(g) subsequent to step (e), removing the support material.

5. The method of claim 2, wherein the support material is not electrically active.

**6.** The method of claim **1**, wherein step (e) comprises:

removing substantially the entire portion of the growth substrate from the device die.

**7.** The method of claim **6**, wherein step (e) comprises:

illuminating the portion of the growth substrate included on the device die with laser light.

**8.** The method of claim **7**, wherein the growth substrate is made of sapphire and the laser light is ultraviolet laser light.

**9.** The method of claim **1**, wherein step (e) comprises:

removing less than the entire portion of the growth substrate from the device die.

**10.** The method of claim **9**, wherein a thickness of the growth substrate on the device die subsequent to step (e) is less than the thickness prior to step (e).

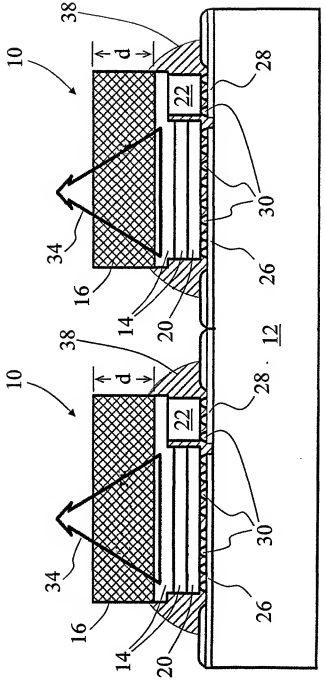



FIG 1A

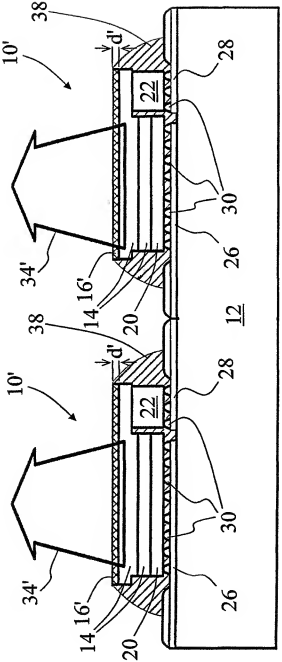
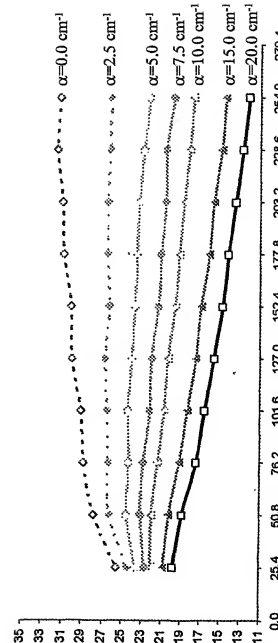



FIG 1B


Light Extraction Fraction
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0.33
0.31
0.29
0.27
0.25
0.23
0.21
0.19
0.17
0.15
0.13
0.11
0.0
25.4
50.8
76.2
101.6
127.0
152.4
177.8
203.2
228.6
254.0
279.4
Substrate Thickness (microns)
α=0.0 cm-1
α=2.5 cm-1
α=5.0 cm-1
α=7.5 cm-1
α=10.0 cm-1
α=15.0 cm-1
α=20.0 cm-1

FIG 2

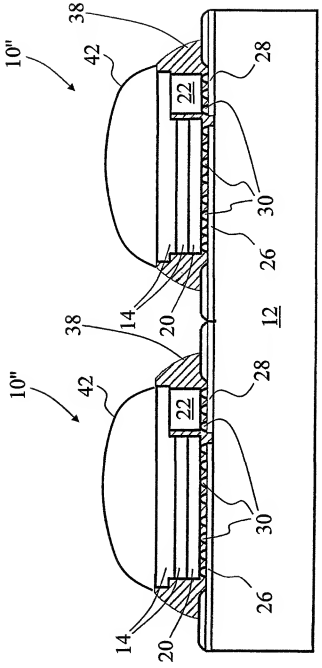


FIG 3

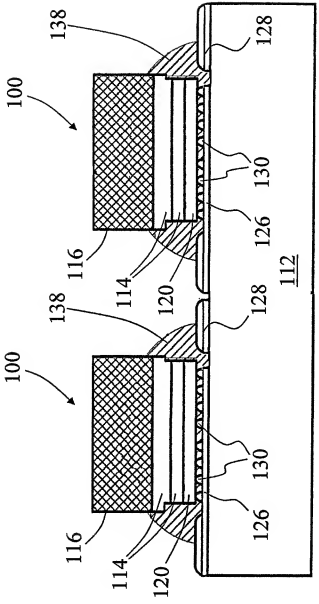
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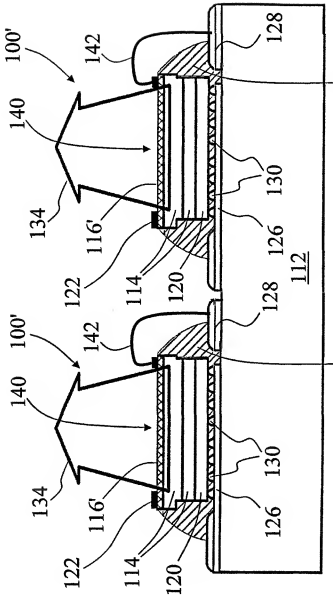
FIG 4A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100'
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126
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128
138

FIG 4B

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
2 August 2001 (02.08.2001)

PCT

(10) International Publication Number
WO 01/56063 A3

(51) International Patent Classification⁷: H01L 21/301, 21/44, 23/02

(21) International Application Number: PCT/US01/02544

(22) International Filing Date: 25 January 2001 (25.01.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/491,456 26 January 2000 (26.01.2000) US

(71) Applicant: TRU-SI TECHNOLOGIES, INC. [US/US]; 657 North Pastoria Avenue, Sunnyvale, CA 94086 (US).

(72) Inventors: SINIAGUINE, Oleg; 1247 Weibel Way, San Jose, CA 95125 (US). HALAHAN, Patrick; 3932 Casanova, San Mateo, CA 94403 (US). SAVASTIOUK, Sergey; 1627 Sparkling Way, San Jose, CA 95125 (US).

(74) Agent: Michael Shenker, Esq.; Skjerven Morrill MacPherson, 25 Metro Drive, Suite 700, San Jose, CA 95110 (US).

(81) Designated States (national): IL, JP, KR, SG.

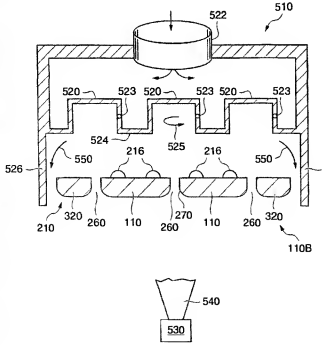
(84) Designated States (regional): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— with international search report

(88) Date of publication of the international search report:
3 January 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: THINNING AND DICING OF SEMICONDUCTOR WAFERS USING DRY ETCH, AND OBTAINING SEMICONDUCTOR CHIPS WITH ROUNDED BOTTOM EDGES AND CORNERS




(57) Abstract: A semiconductor wafer (210) is diced before thinning. The wafer (210) is diced only part of the way through, to form grooves which are at least as deep as the final thickness of each chip to be obtained from the wafer. Then, the wafer is placed into a non-contact wafer holder (510), and the wafer backside is blanket etched with a dry etch, for example, atmospheric pressure plasma etch. The wafer is thinned until the grooves are exposed from the backside. The dry etch leaves the chip's backside smooth. After the grooves have been exposed, the dry etch is continued to remove damage from the chip sidewalls and to round the chip's bottom edges (110E) and corners (110C). As a result, the chip becomes more reliable, and in particular more resistant to thermal and other stresses.

WO 01/56063 A3

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/02544

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H01L 21/301, 21/46, 21/44, 23/02
US CL : 438/113, 114, 460, 461, 462, 463, 464, 706; 257/678
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/113, 114, 460, 461, 462, 463, 464, 706; 257/678

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

JPO, EPO, Dew

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A,P | US 6,176,966 B1 (Tsujimoto et al) 23 January 2001 (23.01.01), Fig.1 | 1-21 |
| A | US 6,004,867 A (Kim et al) 21 December 1999 (21.12.99), Col.5, line 16- Col.6, line 65. | 1-21 |
| A | US 3,991,296 (Kojima et al) 09 November 1976 (09.11.76), col.3, line 47 - Col.4, line49 | 1-21 |
| X | US 3,739,463 (Aird et al) 19 June 1973 (19.06.73), Fig.9 | 20-22 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

| | | | |
|---|---|---|---|
| * | Special categories of cited documents: | "T" | later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention |
| "A" | document defining the general state of the art which is not considered to be of particular relevance | "X" | document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone |
| "E" | earlier document published on or after the international filing date | "Y" | document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art |
| "L" | document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) | "&" | document member of the same patent family |
| "O" | document referring to an oral disclosure, use, exhibition or other means | | |
| "P" | document published prior to the international filing date but later than the priority date claimed | | |

| | |
|---|---|
| Date of the actual completion of the international search<br>30 APRIL 2001 | Date of mailing of the international search report<br>12 JUN 2001 |
| Name and mailing address of the ISA/US<br>Commissioner of Patents and Trademarks<br>Box PCT<br>Washington, D.C. 20231<br>Facsimile No. (703) 305-3230 | Authorized officer<br>DONGHEE KANG<br>Telephone No. (703) 305-9147 |

Form PCT/ISA/210 (second sheet) (July 1998)*

# INTERNATIONAL SEARCH REPORT

Inte...ational application No.
PCT/US01/02544

**Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)**

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

See form PCT/ISA/206, Invitation To Pay Additional Fee's, mailed 24 March 2001. Applicant elected to pay all fee's.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

**Remark on Protest**

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
14 July 2005 (14.07.2005)

PCT

(10) International Publication Number
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(21) International Application Number: PCT/US2004/043201

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(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/532,839 24 December 2003 (24.12.2003) US

(71) Applicant (*for all designated States except US*): **GELCORE LLC** [US/US]; 6180 Halle Drive, Valley View, OH 44125-4635 (US).

(72) Inventors: **SHELTON, Bryon, S.**; 414 William Street, Bound Brook, NJ 08805 (US). **LIBON, Sebastian**; 95 Horatio Street, Apt. 617, New York, NY (US). **ELIASHEVICH, Ivan**; 514 Prospect Street, Maplewood, NJ 07040 (US).

(74) Agent: **MCCOLLISTER, Scott, A.**; Fay, Sharpe, Fagan, Minnich & McKee, LLP, 1100 Superior Avenue, Seventh Floor, Cleveland, OH 44114-2579 (US).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Published:**
— *with international search report*

(88) Date of publication of the international search report:
24 November 2005

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: LASER LIFT-OFF OF SAPPHIRE FROM A NITRIDE FLIP-CHIP

(57) Abstract: In a method for fabricating a flip-chip light emitting diode device, epitaxial layers are deposited on a sapphire growth substrate to produce an epitaxial wafer. A plurality of light emitting diode devices are fabricated on the epitaxial wafer. The epitaxial wafer is diced to generate a device die. The device die is flip chip bonded to a mount. The flip chip bonding includes securing the device die to the mount by bonding at least one electrode of the device die to at least one bonding pad of the mount. Subsequent to the flip chip bonding, the growth substrate of the device die is removed via the application of laser light.

WO 2005/062905 A3

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US04/43201

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H01L 21/00, 33/00
US CL : 438/22, 108
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 438/22, 108

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WEST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| E | US 2005/0023550A (ELIASHEVICH et al) 3 February 2005 (03.02.2005), page 5. | 1-10 |
| A | US 6,280,523A (COMAN et al) 28 August 2001 (28.08.2001), column 9, lines 1-55. | 1-10 |
| A | US 5,376,580A (KISH et al) 27 December 1994 (27.12.1994), columns 10-11. | 1-10 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 12 July 2005 (12.07.2005) | 26 JUL 2005 |
| Name and mailing address of the ISA/US<br>Mail Stop PCT, Attn: ISA/US<br>Commissioner for Patents<br>P.O. Box 1450<br>Alexandria, Virginia 22313-1450<br>Facsimile No. (703) 305-3230 | Authorized officer<br>Alexander G. Ghyka<br>ALEXANDER GHYKA<br>PRIMARY EXAMINER<br>Telephone No. (703) 308-0956 |